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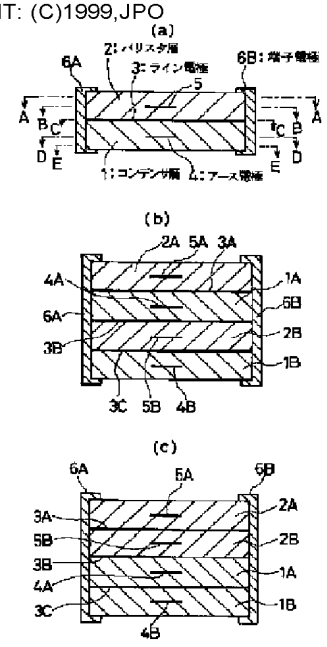
(54) **CHIP TYPE NOISE FILTER**

(57) Abstract:

PROBLEM TO BE SOLVED: To integrate capacitor and varistor functions with each other in a chip type noise filter and miniaturize it, by laminating dielectric and varistor layers via a line electrode, and by inserting a ground electrode horizontally into the dielectric and varistor layers so as to be orthogonal to the line electrode.

SOLUTION: In a chip-type noise filter, only one varistor layer 2 is stacked on only one dielectric layer 1 via a line electrode 3, respective ground electrodes 4, 5 are provided horizontally in the orthogonal direction to the line electrode 3 in the insides of the dielectric and varistor layers 1, 2. On both the end surfaces of the laminated body comprising the dielectric layer 1, the line electrode 3, and the varistor layer 2, terminal electrodes 6A, 6B are provided to bring the layers 1, 2 into electric conudctions to the line electrode 3. Thereby, a small-sized high-performance chip-type noise filter having doubly capacitor and varistor functions can be obtained.



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CLAIMS

[Claim(s)]
[Claim 1]A chip type noise filter, wherein it comes to laminate a dielectric layer and a barista layer via a line electrode and a ground electrode is inserted in the direction which intersects this line electrode at this dielectric layer and a barista layer.
[Claim 2]A chip type noise filter characterized by coming to laminate two or more dielectric layers and barista layers by turns via a line electrode in claim 1.

[Claim 3]A chip type noise filter characterized by coming to laminate a layer which comes to laminate two or more dielectric layers via a line electrode, and a layer which comes to laminate two or more barista layers via a line electrode via a line electrode in claim 1.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to the chip type noise filter which carried out the compound unification of a capacitor function and the barista function.
[0002]
[Description of the Prior Art]Conventionally, generally the noise filter provided in a signal line is considered as the composition which combined the capacitor and the barista's discrete device.
[0003]
[Problem(s) to be Solved by the Invention]In the conventional noise filter, since it combined using a capacitor and a barista's discrete device respectively, a miniaturization was not able to be attained.
[0004]This invention solves the above-mentioned conventional problem, and it aims at providing the chip type noise filter which miniaturized the capacitor function and the barista function by carrying out compound unification.

[0005]
[Means for Solving the Problem]A ground electrode is inserted in this dielectric layer and a barista layer so that it may come to laminate a dielectric layer and a barista layer via a line electrode and a chip type noise filter of this invention may intersect this line electrode.
[0006]In a chip type noise filter of this invention, since the compound unification of the barista who consists of a capacitor, a barista layer, and an electrode which consist of a dielectric layer and an electrode is carried out, a miniaturization of a noise filter can be attained.
[0007]A chip type noise filter of this invention can be easily manufactured by laminating a ceramic green sheet of dielectric materials, and a ceramic green sheet of barista material via an electrode, and really calcinating them.

[0008]laminating two or more dielectric layers and barista layers by turns via a line electrode in a chip type noise filter of this invention -- or, A filtering function can be improved by laminating a layer which laminated two or more dielectric layers via a line electrode, and a layer which laminated two or more barista layers via a line electrode via a line electrode.

[0009]
[Embodiment of the Invention]With reference to drawings, an embodiment of the invention is described in detail below.
[0010]The sectional view in which - (b) shows an embodiment of the invention, and drawing 1 (a) drawing 2 (a) - (d) are sectional views which meet the A-A line, the B-B line, C-C line, and D-D line of drawing 1 (a) respectively (however, in drawing 2, the terminal electrode has omitted the graphic display.). Drawing 3 is a representative circuit schematic of the chip type noise filter of drawing 1 (a).
[0011]The chip type noise filter shown in drawing 1 (a) laminates the dielectric layer 1 and one layer of barista layers 2 at a time via the line electrode 3, and the ground electrodes 4 and 5 are formed in the direction which intersects perpendicularly with the inside of the dielectric layer 1 and the barista layer 2 with the line electrode 3, respectively. The terminal electrodes 6A and 6B are formed in the both-ends side of the layered product of this dielectric layer 1, the line electrode 3, and the barista layer 2 so that it may flow in the line electrode 3, and the terminal electrode (not shown) which flows in the ground electrodes 4 and 5 is provided in the side of the layered product.
[0012]As this chip type noise filter is shown in drawing 3, the barista V grounded with the ground electrode 5 is connected with the capacitor C grounded with the ground electrode 4 by the line electrode 3, A good noise filter function can be obtained by connecting with a circuit with the terminal electrodes 6A and 6B.
[0013]The chip type noise filter shown in drawing 1 (b) laminates by turns the dielectric layers 1A and 1B in which the ground electrodes 4A and 4B were formed respectively, and the barista layer 2A and 2B in which the ground electrodes 5A and 5B were formed respectively via the line electrodes 3A and 3B and 3C.

[0014]The chip type noise filter shown in drawing 1 (c), The barista layer 2A and 2B in which the dielectric layers 1A and 1B in which the ground electrodes 4A and 4B were formed respectively were laminated via the line electrode 3A, and the ground electrodes 5A and 5B were formed respectively are laminated via line electrode 3C, and these layers are laminated via the line electrode 3B.

[0015]If it is a chip type noise filter shown in these drawing 1 (b) and (c), high capacity and the chip type noise filter of high varistor voltage are realizable.
[0016]The chip type noise filter of such this invention, It can manufacture easily by forming a ground electrode or a line electrode in a necessary part, respectively, laminating the ceramic green sheet of dielectric materials, and the ceramic green sheet of barista material, calcinating a layered product, and forming a terminal electrode in a necessary part after that.
[0017]As dielectric materials, relaxer materials, such as Pb(Mg, Nb) O3-PbTiO3, BaTiO3+ textile-glass-yarn material, etc. can be used, for example. As a barista material, a ZnO system, a SrTiO3 system, etc. can be used, for example.

[0018]
[Example]An example is given to below and this invention is more concretely explained to it.
[0019]As Example 1 and 2 dielectric materials, use lead relaxer system material (presentation-b(Mg, Nb) O3-PbTiO3 system), and the material (presentation: ZnO-Bi2O3 system) which uses ZnO as the main ingredients is used as a barista material, The chip type noise filter shown in drawing 1 (a) was produced.

[0020]Into the above-mentioned dielectric materials and barista material, respectively First, an organic binder, a solvent, The dispersing agent and the plasticizer were added, it was considered as slurry form, and the 30-50-micrometer-thick dielectric ceramic green sheet and the barista ceramic green sheet were produced with the doctor blade method using this slurry.

[0021]After sticking a dielectric ceramic green sheet by pressure by the pressure of 2 t/cm2 by 70 ** of five-sheet piles, it formed by printing an Ag/Pd paste to one field and drying as a ground electrode, to it. Two or more dielectric ceramic green sheets are laminated, and it is similarly stuck to this ground electrode forming face side by pressure.
Then, the line electrode was formed by printing an Ag/Pd paste to one field and drying to it.

[0022]After laminating and sticking two or more barista ceramic green sheets to this line electrode formation face by pressure and forming a ground electrode in it like the above, five barista ceramic green sheets were laminated and stuck by pressure. And after carrying out the de binder of this layered product, it calcinated at 1100 ** for 2 hours.
[0023]After plastering the obtained sintered compact so that it may flow through an Ag/Pd paste in a line electrode and a ground electrode, respectively, it prints at 750 ** and a terminal electrode is formed.
Then, nickel plating and solder plating were performed and it was considered as the chip type noise filter.

[0024]The width of the line electrode formed the width of 0.64 mm and a ground electrode in 0.7 mm, respectively. The thickness between layers of the obtained chip type noise filter was as being shown in Table 1.
[0025]When the characteristic of the obtained chip type noise filter is investigated, as shown in Table 1, it has the characteristic good as a noise filter.
[0026]
[Table 1]

実施例	1	2
層間厚み※ (μm)	60	90
容量(nF)	1.00	0.68
バリスタ電圧	17	25

※コンデンサ部全体及びバリスタ部全体

[0027]
[Effect of the Invention]According to the chip type noise filter of this invention, the small and highly efficient chip type noise filter which combines a capacitor function and a barista function is provided as explained in full detail above.

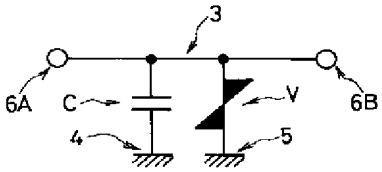
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a sectional view showing the embodiment of the chip type noise filter of this invention.
[Drawing 2]It is a sectional view of each part of the chip type noise filter of drawing 1 (a).
[Drawing 3]It is a representative circuit schematic of the chip type noise filter of drawing 1 (a).
[Description of Notations]
1, 1A, and 1B Dielectric layer
2, 2A, and 2B Barista layer

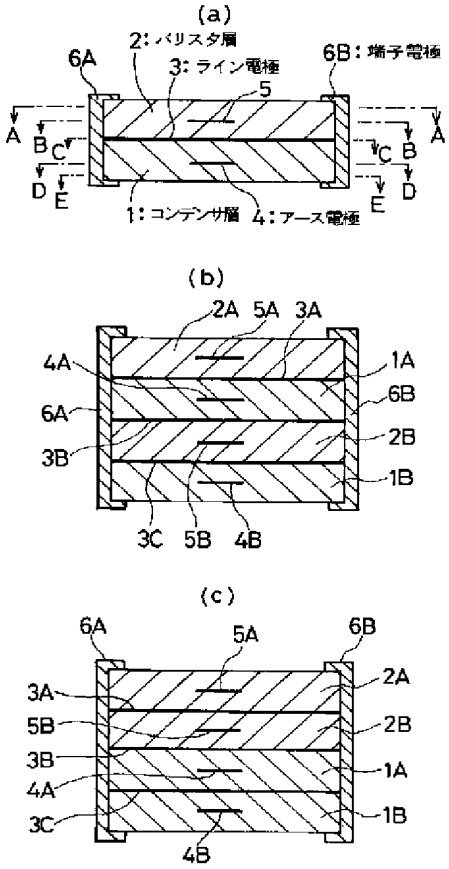
3, 3A, 3B, and 3C Line electrode
4, 4A, 4B, 5, 5A, 5B ground electrode
6A and 6B Terminal electrode

DRAWINGS

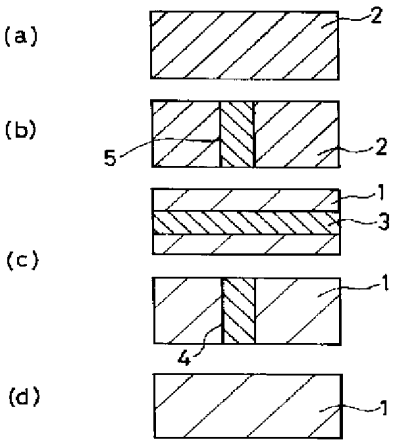
[Drawing 3]



[Drawing 1]



[Drawing 2]


(a)
2
(b)
5
2
1
3
(c)
1
4
(d)
1